REMARKS

Favorable reconsideration of the application is respectfully requested in light of the amendments and remarks herein.

Upon entry of this amendment, claims 1-13 and 49-61 will be pending. By this amendment, claims 1 and 49 have been amended. No new matter has been added.

§112 Rejection of Claims 1-13 and 49-61

In Section 2 of the Office Action, claims 1-13 and 49-61 stand rejected under 35 U.S.C. § 112, first paragraph. Specifically, claims 1 and 48 have been rejected for reciting new matter in stating "concurrent operations of comparison, absolute value computation, and selection in log likelihood computations." It appears that claims 1 and 49, rather than claims 1 and 48, contain this language. Claims 1 and 49 have been amended to address the rejection. Specifically, claim 1 has been amended to state "wherein comparison operations within the path selecting means and absolute value computation within the absolute value selecting means are carried out concurrently in log likelihood computations, and selection processing operations performed within the path selecting means and absolute value selecting means are carried out concurrently in log likelihood computations." This limitation is disclosed in the Specification, page 82, lines 1-7, and is stated as follows: "the processing operations of the comparator circuits 131, 132, 133, 134, 135, 136 and those of the absolute value computation circuits 161, 162, 163, 164, 165, 166 are carried out concurrently along with the processing operations of the selectors 137, 139, 140, 191, 192 and those of the selectors 138, 141, 193. Thus, the delay of the addition/comparison/selection circuit 120 is smaller than that of the addition/comparison/selection 60."

Claim 49 has been similarly amended.

Accordingly, it is submitted that the rejection of claims 1-13 and 49-61 based upon 35

U.S.C. §112 has been obviated and withdrawal thereof is respectfully requested.

§ 101 Rejection of Claims 49-61

In section 4 of the Office Action, claims 49-61 stand rejected under 35 U.S.C. 101

because the claimed invention is directed to non-statutory subject matter. Claims 49-61 have

been amended to address the rejection.

Accordingly, it is submitted that the rejection of claims 49-61 based upon 35 U.S.C. §101

has been obviated and withdrawal thereof is respectfully requested.

§ 103 Rejection of Claims 1-3 and 49-51

In Section 5 of the Office Action, claims 1-3 and 49-51 stand rejected under 35 U.S.C.

§103(a) as being unpatentable over Van Stralen *et al.* (U.S. Patent 6,304,996 B1; hereinafter

referred to as "Van Stralen") in view of Yamanaka *et al.* (U.S. Patent 6,330,684 B1; hereinafter

referred to as "Yamanaka"). Claims 1 and 49 have been amended to address the rejection.

In the Background section of the Specification, it was stated that "[BCJR] describes an

algorithm for minimizing symbol error rates when decoding predetermined codes such as

convolutional codes. ... The BCJR algorithm is designed to output not each symbol but the

likelihood of each symbol as a result of decoding operation. Such an outputs is referred to as

soft-output.." *Background of the Specification, page 1, lines 14-20.* "However, the BCJR

algorithm is accompanied by a problem that it involves a large volume of computational

operations because it requires ... directly hold[ing] probabilities as values to be used for

computations and employ multiplications. As an attempt for reducing the volume of

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computational operations, [an article] ... proposes Max-Log-MAP Algorithm and Log-MAP

Algorithm (... referred to as Max-Log-BCJR algorithm and Log-BCJR algorithm respectively

hereinafter). ... With the Max-Log-BCJR algorithm, the probabilities α_t, β_t and γ_t are expressed

in terms of natural logarithm so that the multiplications for determining the probabilities are

replaced by a logarithmic addition ... and the logarithmic addition is approximated by a

logarithmic maximizing operation ..." *Background of the Specification, page 6, line 17 to page*

7, line 10.

"As pointed out above, since the Max-Log-BCJR algorithm does not involve any

multiplications, it can greatly reduce the volume of computational operations if compared with

the BCJR algorithm. ... The Log-BCJR algorithm is devised to improve the accuracy of

approximation of the Max-Log-BCJR algorithm. More specifically, in the Log-BCJR algorithm,

a correction term is added to the addition of probabilities ... so that the sum of the addition ...

may represent a more accurate logarithmic value. The correction is referred to as log-sum

correction hereinafter." *Background of the Specification, page 10, lines 2-11.*

"These log-sum correction methods are developed by putting stress on the performance

of the algorithm in terms of accurately determining the value of the correction term. However,

they are accompanied by certain problems including a large circuit configuration and slow

processing operations." *Background of the Specification, page 13, line 18 to page 14, line 1*

(emphasis added). "Thus, while various methods have been discussed for the purpose of log-

sum correction, all of them still have something to be improved. ... Not only the log-sum

correction but also the above described operation of determining the maximum value gives rise

to the problem of delay when determining the maximum likelihood path to baffle the efforts for

realizing high speed decoding." *Background of the Specification, page 14, line 19 to page 15,*

line 3 (emphasis added).

To address the above-described problems of the conventional decoders in implementing

the BCJR technique, embodiments of the present invention provide a capability for the maximum

likelihood decoder to provide <u>concurrent computations</u> of log likelihoods, wherein the path

selection means operates to generate corrections to the probability of the particular state of the

Trellis diagram using at least two paths, one path showing a maximum likelihood and another

path showing a second maximum likelihood, from at least three paths in the Trellis diagram.

This configuration provides a faster log-sum correction processing than the configurations

implemented in the conventional decoders. *See Specification, pages 15-16.*

For example, the structure of decoder claim 1, as presented herein, includes:

"*a first probability computing means* for computing a logarithm of branch
metric (γ), which is a logarithm of probability of a particular branch of a
Trellis diagram, computed only based on the knowledge of input and
output symbols associated with the particular branch;

a second probability computing means for computing a logarithm of forward
state metric (α), which is a logarithm of probability of a particular state of
the Trellis diagram, given the probabilities of states at previous time
instances;

a third probability computing means for computing a logarithm of backward
state metric (β), which is a logarithm of probability of the particular state
of the Trellis diagram, given the probabilities of states at future time
instances,

> <u>wherein each of said second probability computing means and said third
> probability computing means includes</u>

a path selection means, said path selection means including:

> *a plurality of comparator circuits* to perform comparison operation,

> *a plurality of selectors* to perform selection operation; and

an absolute value selecting means, said absolute value selecting means
including:

> *a plurality of absolute value computation circuits* to perform absolute
> value computation, and

> *a plurality of selectors* to perform selection operation,

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wherein comparison operations within the path selecting means and
absolute value computation within the absolute value selecting means
are carried out concurrently in log likelihood computations, and
selection processing operations performed within the path selecting
means and absolute value selecting means are carried out concurrently
in log likelihood computations, and

wherein said absolute value data selecting means <u>compares said computed
absolute value data to determine which is larger on the basis of
information on the outcome of comparison obtained by a plurality of
said comparator circuits</u>, and

wherein said path selection means operates to generate corrections to said
probability of the particular state of the Trellis diagram using at least
two paths, one path showing a maximum likelihood and another path
showing a second maximum likelihood, from at least three paths in the
Trellis diagram; and

a soft-output determining means for determining a log soft-output
logarithmically expressing a soft-output in each time slot, given said
forward and backward state metrics as well as said branch metric."

(emphasis added)

In summary, claim 1 generally recites the elements in Figure 9 with second and third

probability computing means including elements of a path selection means and absolute value

selecting means illustrated in Figure 27. The path selection means of claim 1 includes second

and third probability computing means, wherein <u>each of said second probability computing

means and said third probability computing means includes a path selection means</u>, said path

selection means including: a plurality of comparator circuits to perform comparison operation, a

plurality of selectors to perform selection operation; <u>and an absolute value selecting means</u>, said

absolute value selecting means including: a plurality of absolute value computation circuits to

perform absolute value computation, and a plurality of selectors to perform selection operation.

Specification, Fig. 27 (emphasis added). Further, comparison operations within the path

selecting means and absolute value computation within the absolute value selecting means are

carried out concurrently in log likelihood computations, and selection processing operations performed within the path selecting means and absolute value selecting means are carried out concurrently in log likelihood computations. *Specification, page 82, lines 1-7.* Further, <u>said absolute value data selecting means compares absolute value data computed by said absolute value computation circuits of said absolute value selecting means to determine which is larger on the basis of information on the outcome of comparison obtained by a plurality of comparator circuits of the path selecting means</u>. *See Specification, page 70, lines 12-19 (emphasis added).*

It is submitted that Van Stralen and Yamanaka, individually or in combination, fail to teach or disclose a decoder, as described in amended claim 1, including first and second probability computing means, <u>wherein each of said second probability computing means and said third probability computing means includes *a path selection means,*</u> a path selection means, said path selection means including: a plurality of comparator circuits to perform comparison operation, a plurality of selectors to perform selection operation; <u>and *an absolute value selecting means,*</u> said absolute value selecting means including: a plurality of absolute value computation circuits to perform absolute value computation, and a plurality of selectors to perform selection operation, *wherein* <u>comparison operations</u> within the path selecting means <u>and absolute value computation</u> within the absolute value selecting means *are carried out concurrently* in log likelihood computations, <u>and selection processing operations performed within the path selecting means and absolute value selecting means</u> *are carried out concurrently* in log likelihood computations, and <u>wherein said absolute value data selecting means compares said computed absolute value data to determine which is larger on the basis of information on the outcome of comparison obtained by a plurality of said comparator circuits</u>. Therefore, it is maintained that

Van Stralen and Yamanaka, individually or in combination fail to teach or suggest all the limitations of claim 1.

Based on the foregoing discussion, it is maintained that claim 1 should be allowable over Van Stralen and Yamanaka. Since claim 49, as amended herein, closely parallels, and includes substantially similar limitations as recited in, claim 1, claim 49 should also be allowable over Van Stralen and Yamanaka. Since claims 2-3 and 50-51 depend from claims 1 and 49, respectively, claims 2-3 and 50-51 should also be allowable over Van Stralen and Yamanaka.

Accordingly, it is submitted that the rejection of claims 1-3 and 49-51 based upon 35 U.S.C. §103(a) has been overcome by the present remarks and withdrawal thereof is respectfully requested.

§ 103 Rejection of Claims 4, 5, 52, and 53

In Section 6 of the Office Action, claims 4, 5, 52, and 53 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Van Stralen and Yamanaka in view of Benedetto *et al.* (S. Benedetto, D. Divsalar, G. Montorsi, and F. Pollara, Soft-Output Decoding Algorithms in Iterative Decoding of Turbo Codes, TDA Progress Report 42-124, NASA Code 315-91-20-20-53; hereinafter referred to as "Benedetto").

Based on the foregoing discussion regarding claims 1 and 49, and since claims 4-5 and 52-53 depend from claims 1 and 49, claims 4-5 and 52-53 should be allowable over Van Stralen and Yamanaka. Further, Benedetto was cited for teaching the specific use of the computed absolute values being compared for magnitude. Thus, it is maintained that Van Stralen, Yamanaka, and Benedetto fail to teach or suggest all the limitations of claims 4-5 and 52-53.

Accordingly, it is submitted that the rejection of claims 4-5 and 52-53 based upon 35 U.S.C. §103(a) has been overcome by the present remarks and withdrawal thereof is respectfully requested.

§ 103 Rejection of Claims 6, 9, 10, 12, 13, 54, 57, 58, 60, and 61

In Section 6 of the Office Action, claims 6, 9, 10, 12, 13, 54, 57, 58, 60, and 61 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Van Stralen, Yamanaka, and Benedetto in view of XP-000888685 ("Simplified Log-Map Algorithm", Research Disclosure, Kenneth Mason Publications, Hampshire, GC, No. 421, May 1999, Page 612, ISSN: 0374-4353; hereinafter referred to as "XP-000888685").

Based on the foregoing discussion regarding claims 1 and 49, and since claims 6, 9, 10, 12, 13, 54, 57, 58, 60, and 61 depend from one of claims 1 and 49, claims 6, 9, 10, 12, 13, 54, 57, 58, 60, and 61 should be allowable over the combination of Van Stralen, Yamanaka, and Benedetto. Further, the reference XP-000888685 was only cited for teaching that $B=4=2^2$. Therefore, it is maintained that Van Stralen, Yamanaka, Benedetto, and XP-000888685, in combination or individually, fail to teach or suggest all the limitations of claims 6, 9, 10, 12, 13, 54, 57, 58, 60, and 61.

Accordingly, it is submitted that the rejection of claims 6, 9, 10, 12, 13, 54, 57, 58, 60, and 61 based upon 35 U.S.C. §103(a) has been overcome by the present remarks and withdrawal thereof is respectfully requested.

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<u>Conclusion</u>

In view of the foregoing, entry of this amendment, and the allowance of this application

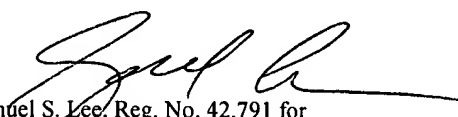with claims 1-13 and 49-61 are respectfully solicited.

In regard to the claims amended herein and throughout the prosecution of this

application, it is submitted that these claims, as originally presented, are patentably distinct over

the prior art of record, and that these claims were in full compliance with the requirements of 35

U.S.C. §112. Changes that have been made to these claims were not made for the purpose of

patentability within the meaning of 35 U.S.C. §§101, 102, 103 or 112. Rather, these changes

were made simply for clarification and to round out the scope of protection to which Applicant is

entitled.

In the event that additional cooperation in this case may be helpful to complete its

prosecution, the Examiner is cordially invited to contact Applicant's representative at the

telephone number written below.

The Commissioner is hereby authorized to charge any insufficient fees or credit any

overpayment associated with the above-identified application to Deposit Account 50-0320.

Respectfully submitted,

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